SYLLABUS

1. **Course name:** Digital IC Design Lab Using HDL
2. **Course code:** PRDS320663
3. **Credits:** 2 (0/6/12)
   Duration: 15 weeks (0 theories + 6 laboratories + 12 self-studying/week)
4. **Instructors:**
   1- Nguyen Dinh Phu, MEng
   2- Nguyen Tan Nhu, MEng
   3- Truong Thi Bich Nga, MEng
5. **Course conditions**
   Prerequisites: Digital IC Design Using HDL, Digital Systems
   Corequisites: Digital IC Design Using HDL, Digital Systems
6. **Course description**

This course instruct students the whole process of combinational and sequential circuit designs using VHDL. The students firstly design digital IC systems in VHDL hardware description languages on EDA software supported by Xilinx and Altera. Finally, the functions of the designed digital systems are verified by simulation software before being tested on FPGA platforms.

7. **Course Goals**

Goals	***Goal description*** *(This course provides students:)*	**ELOs**
G1	Basic knowledge of digital IC designs	01 (M)
G2	An ability to analyze, prototype, and describe digital systems	02 (H)
G3	An ability to use up-to-date software design tools in order to implement the basic digital system designs in real FPGAs	03 (H)
G4	An ability to use English in reading the documents for pre-labs and reports related to digital technologies	05 (M) 07 (M)
G5	An ability to analyze and design digital circuits	11 (H)

** Note: High: H; Medium: M; Low: L*

8. **Course Learning Outcomes (CLOs)**

CLOs		***Description*** *(After completing this course, students can have:)*	**Outcome**
G1	G1.1	The ability to configure FPGA kits in testing the digital circuit functions	01
	G1.2	The ability to identify the real process of digital IC design using VHDL	01

G2	G2.1	The ability to apply appropriately different kinds of digital circuits in design using VHDL	02
	G2.2	The ability to analyze and design frequency divider circuits	02
G3	G3.1	The ability to use EDA software to design digital circuits	03
	G3.2	The ability to use simulation software to verify the functions of digital circuits	03
G4	G4.1	The ability to use English to read datasheets of pre-designed ICs in the markets	05
	G4.2	The ability to write pre-labs, reports and representation	07
G5	G5.1	The ability to design counter circuits with multiple functions displayed on LED, 7 segment LED, and LCD	11
	G5.2	The ability to design digital circuits interfacing with temperature sensors and SRAM displayed on LCD	11
	G5.3	The ability to design interfacing IC transferring data with PC in the UART and I2C protocols	11

9. Study materials

- Textbooks:

[1] Nguyen Đinh Phu, *The Lessons of Digital IC Design Lab using VHDL*, HCM City Univsersity of Technolgoy and Education, 2016.

- References:

[2] Pong P. Chu, *FPGA Prototyping by VHDL Examples,* Wily, Prentice Hall 2010

10. Student Assessments

- Grading points: 10

- Planning for students assessment is followed:

Type	Contents	Linetime	Assessment techniques	CLOs	Rates (%)
Quizes					**30**
Test 1	Basic knowledge of how to use EDA software and FPGA kits, pre-labs	Week 2	Online	G1.1 G1.2 G4.2	5
Test 2	Basic structures of VHDL used to design combinational circuits	Week 3	Online	G2.1 G2.2	5
Test 3	Basic sequential circuit design displayed on LEDs	Week 4, Week 5	Online	G2.1 G2.2	5
Test 4	Counter circuits displayed on 7 segment LEDs, pre-labs	Week 7, Week 8	Online	G2.1 G2.2 G4.1 G4.2 G5.1	5
Test 5	Counter circuits displayed on LCDs , pre-labs	Week 11, Week 12	Online	G2.1 G2.2 G4.1 G4.2 G5.1	5

				G5.2	
Test 6	RAM IC controllers connected with PC through the UART protocol	Week 13, Week 14	Online	G5.1 G5.2 G5.3	5
Laboratory assignment tests					**70**
Test 1	Simple sequential circuits using buttons and switches as inputs and displayed on LEDs	Week 6	Computers and FPGA kits	G3.1 G3.2 G5.1	20
Test 2	Advanced sequential circuits using buttons and switches as inputs and displayed on 7 segnment LEDs	Week 10	Computers and FPGA kits	G3.1 G3.2 G5.1 G5.2	20
Test 3	RAM, I2C, temperature, and humidity IC controllers displayed on LCDs	Week 15	Computers and FPGA kits	G3.1 G3.2 G5.1 G5.2 G5.3	30

11. Course details:

Weeks	Contents	CLOs
1, 2	***Chapter 1:*** **<OVERVIEWS OF XILINX FPGA KITS>**	
	A/ **Contents and teaching methods***:* **Contents:** 1.1 Overviews of the Xilinx FPGA kit 1.2 Basic functions of each components in the kit **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1
	B/ **Self-study contents**: 1.3 Homework	
3, 4	***Chapter 2:*** **<OVERVIEWS OF XILINX ISE DESIGN SUIT 14.7>**	
	A/ **Contents and teaching methods***:* **Contents:** 2.1 Starting the Xilinx ISE Design Suit program 2.2 Editing a VHDL program in ISE Webpack 2.3 Synthesis the VHDL program in ISE Webpack 2.4 Pin planing for input and output signal in the VHDL programs 2.5 FPGA structure configuration **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.2

	***B/* Self-study contents**: 2.6 Homework	
5, 6	***Chapter 3:* < COMBINATIONAL CIRCUIT DESIGN >**	
	A/* Contents and teaching methods:* **Contents:** 3.1 Overviews 3.2 Decoders 3.3 Encoders 3.4 Multiplexers 3.5 Demultiplexers 3.6 7 segment LED decoders 3.7 Binary adders 3.8 Binary-to-BCD decoders 3.9 BCD-to-7-segment decoder **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2
	***B/* Self- study contents**: *(6)* 3.10 Homework	
2	***Chapter 4:* < SEQUENTIAL CIRCUIT 1: DIVIDERS, BINARY COUNTERS, AND FSM MODELS >**	
	A/* Contents and teaching methods:* **Contents:** 4.1 Overviews 4.2 General synchronous circuits 4.3 Dividers 4.4 Pulse generators 4.5 Binary counters displayed on LEDs 4.6 Random synchrnous circuits 4.7 Button and switch debouncers 4.8 Ring and Johnson counters 4.9 Blocking diagram design orientation **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2
	***B/* Self- study contents**: 4.10 Homework	
3	***Chapter 5:* <SEQUENTIAL CIRCUIT 2: COUNTER DESIGNS DISPLAYED ON 7 SEGMENT LEDS>**	

	A/* Contents and teaching methods:* **Contents:** 5.1 Overviews 5.2 Counters displayed on 7 segment LEDs – method 1 5.3 Counters displayed on 7 segment LEDs – method 2 5.4 Binary counters 5.6 Applications of counters – Digital clocks **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2 G4.1 G4.2 G5.1
	***B/* Self- study contents**: 5.7 Homework	
4	***Chapter 6:* < LCD DISPLAY CONTROLLER >**	
	A/* Contents and teaching methods:* **Contents:** 6.1 Overviews of LCD 6.2 LCD controller with 8-bit interface 6.3 Character displayer with 8-bit interface 6.4 Counters displayed on LCD 6.5 Digital clocks displayed on LCD 6.6 Character displayer with 4-bit interface **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2 G4.1 G4.2 G5.1 G5.2
	***B/* Self- study contents**: 6.7 Homework	
5	***Chapter 7:* < RAM CONTROLLER DESIGNS >**	
	A/* Contents and teaching methods:* **Contents:** 7.1 Overviews 7.2 SRAM configurations 7.3 SRAM on the FPGA kit 7.4 RAM controller designs 7.5 Applications of RAM controllers **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2 G4.1 G4.2 G5.1 G5.2

	***B/* Self- study contents**: 7.6 Homework	
6	***Chapter 8:* < DATA TRANSFERING CIRCUITS>**	
	A/* Contents and teaching methods:* **Contents:** 8.1 Overviews 8.2 UART reveivers 8.3 UART transmitters 8.4 UART transceivers 8.5 PC-FPGA interface using the UART protocol **Teaching methods**: + Presentation + Formulation + Frequent instruction	G1.1 G1.2 G2.1 G2.2 G3.1 G3.2 G4.1 G4.2 G5.1 G5.2 G5.3
	***B/* Self- study contents**: 8.6 Homework	

12. Learning ethics:

- Home assignments and projects must be done by the students themselves. Plagiarism found in the assessments will get zero point

13. First approved date: August 01 2012

14. Approval level:

Dean	**Department**	**Instructor**

15. Syllabus updated process

1st time: Updated content dated	Instructors Nguyen Dinh Phu
2st time: Updated content dated	Head of department